

HyperTransport in a Very High Performance Integrated Multiprocessor

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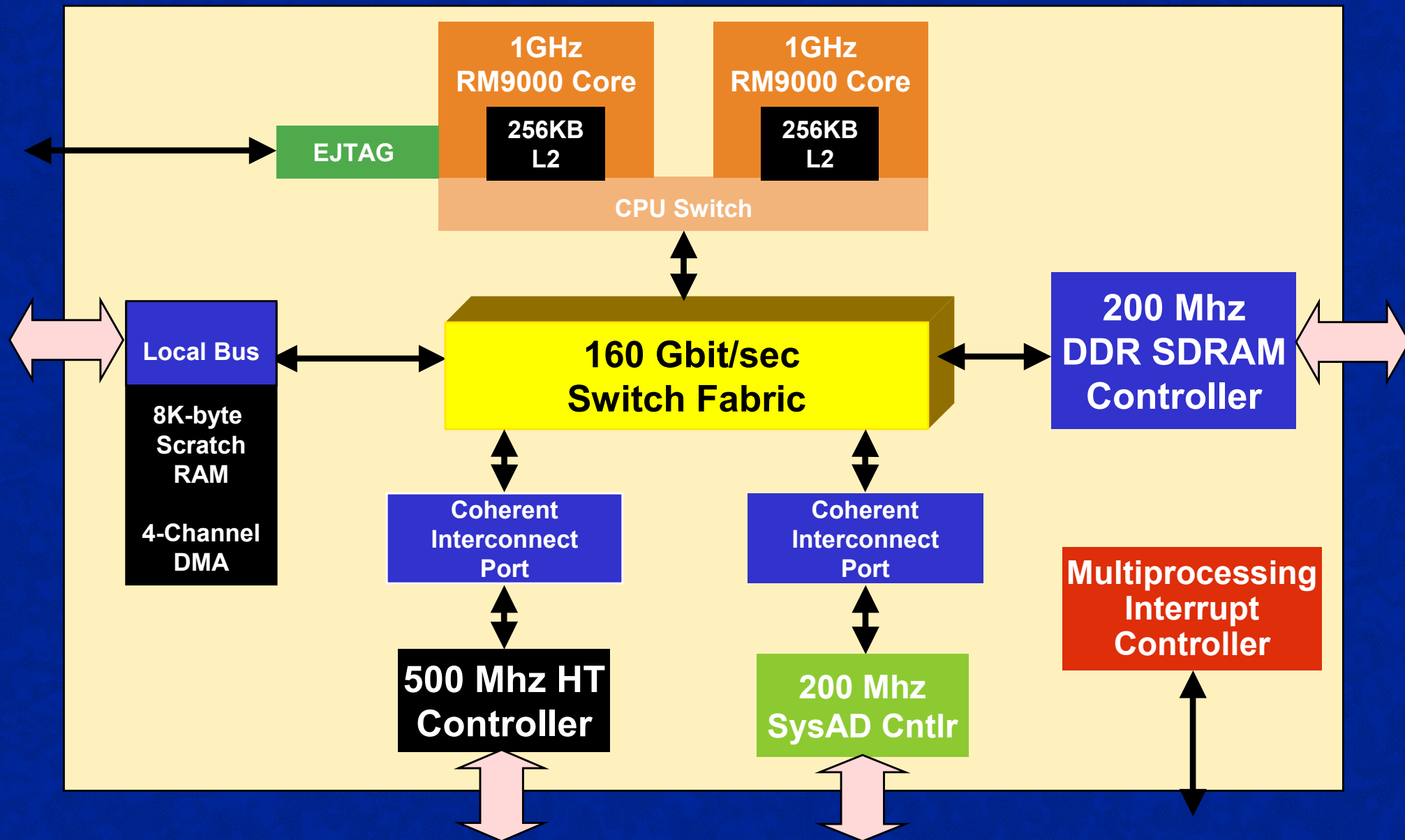


Platform
Conference
Direction • Design • Perspective • Analysis

Agenda

- **RM9000x2 Integrated Multiprocessor Architecture**
 - High Performance CPU Subsystem Requires High Performance I/O
- **Why HyperTransport?**
 - Features and Competitive Comparison
- **System Solutions Using HyperTransport**
- **Summary**

RM9000x2 Block Diagram



RM9000x2 I/O Bus Requirements

- **Must Provide I/O Performance to Scale with Dual Gigahertz CPUs**
 - Networking Market Requires High Performance in both Processing and I/O
 - Bandwidth Needs to Utilize RM9000x2 160 Gbit/sec Switch Fabric
 - Must Support Advanced Features of RM9000x2, such as DMA of Packet Headers into L2 Cache
- **Companion Chip Availability**
- **Scalability**

Which I/O Bus?

- **Two I/O Bus Standards Offer “In the Box” Solution**
 - HyperTransport
 - Rapid I/O
- **Infiniband a Complementary “Out of the Box” Solution**

PCI Compatibility

- **HyperTransport was Designed to be a Superset of PCI**
 - **Maintains PCI Register Format and Definitions**
 - **Maintains PCI Ordering Semantics**
 - **Rules to Prevent Deadlock**
 - **PCI Bridge Architectures Supported**
- **Rapid IO Wasn't Designed with PCI Legacy in Mind**

HyperTransport/ Rapid IO Similarities

- **Both HyperTransport and Rapid IO Provide**
 - “In the Box” Solution
 - Low Pin Count
 - Source Synchronous Unidirectional Parallel Bus Architecture
 - DDR Clocking
 - Support for Memory Mapped Distributed Memory
 - 3 Protocol Layer Packet Format

HT/ RIO Differences

	HT	RIO
Based on PCI	Yes	No
Bus Widths Supported (Each Direction)	2,4,8,16,32	8,16
Max Bus BW (1 GHz)	100 Gbit/sec	50 Gbit/sec
Efficiency (32 Byte Packets)	80%	50%
Max Packet Size (bytes)	64	256
Flow Control	Credit (Most Effective)	Credit, Throttle, Retry
Part Available	Yes	No
RTL Available	Yes	?

HyperTransport Companion Chip Momentum

- **API Networks**

- Currently Sampling HT-PCI Bridge
- Additional HyperTransport Chips Available End of 2001



- **Marvel/Galileo**

- Developing Family of Networking Chips using HyperTransport



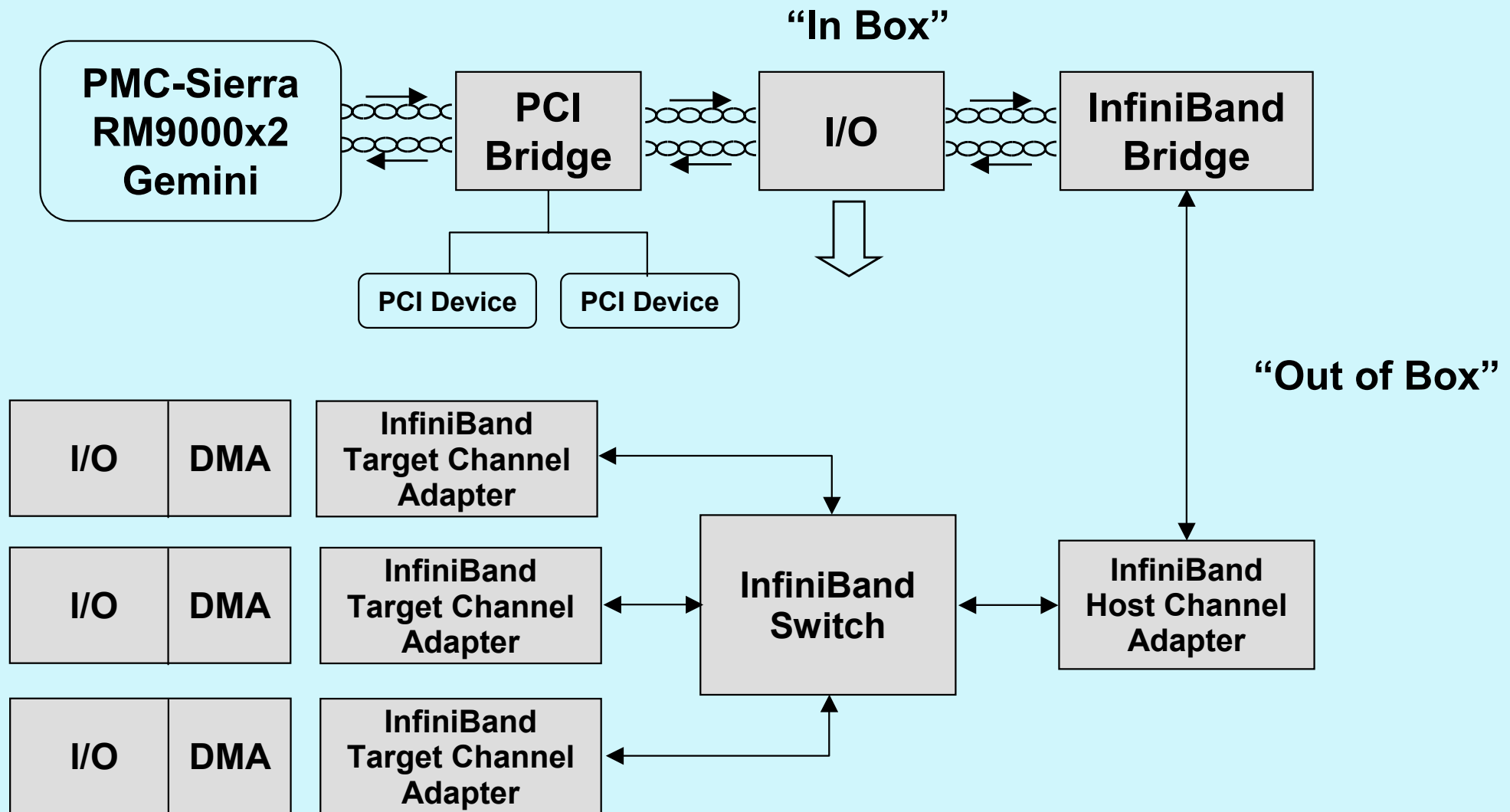
- **FPGA Support**

- Xilinx and Altera



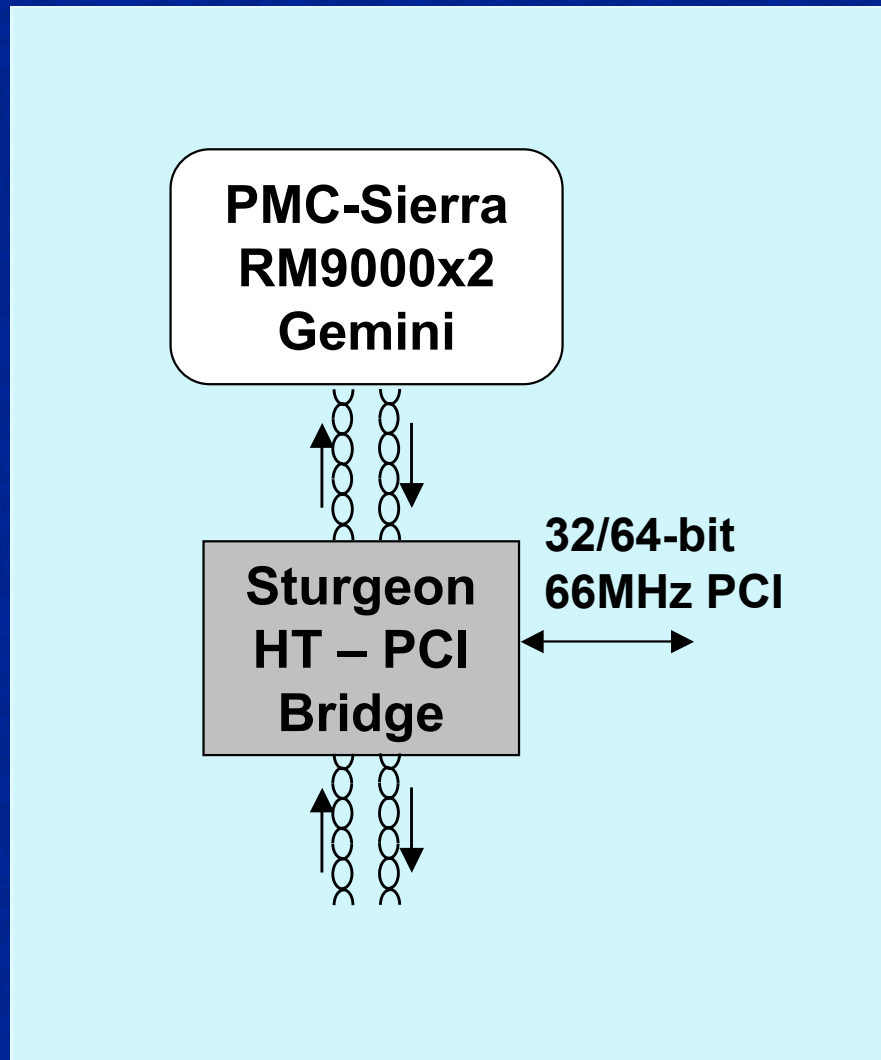
- **Additional Companion Chip Support to be Announced Soon**

Example HyperTransport System



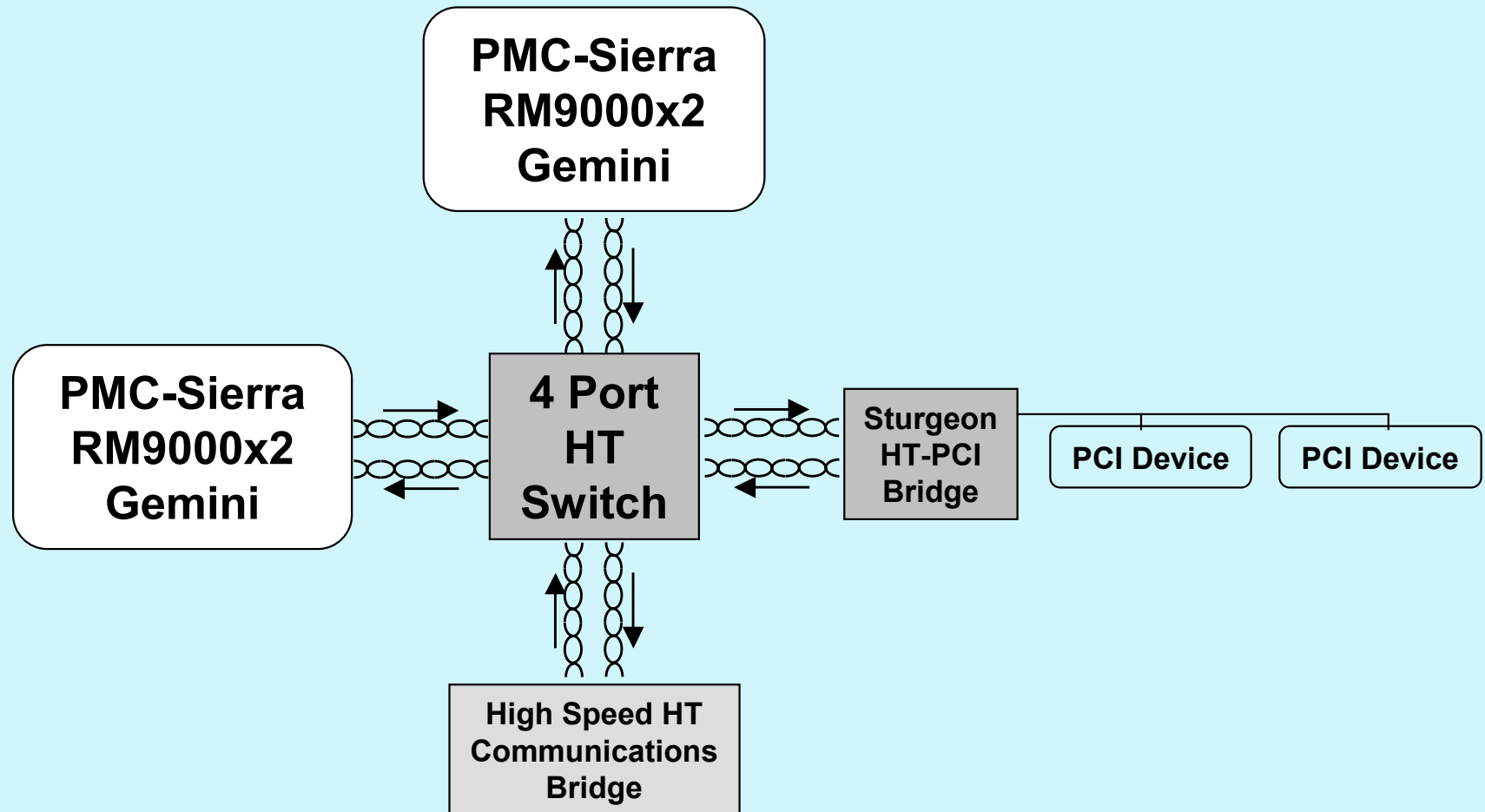
API Networks Sturgeon

HyperTransport to PCI Bridge

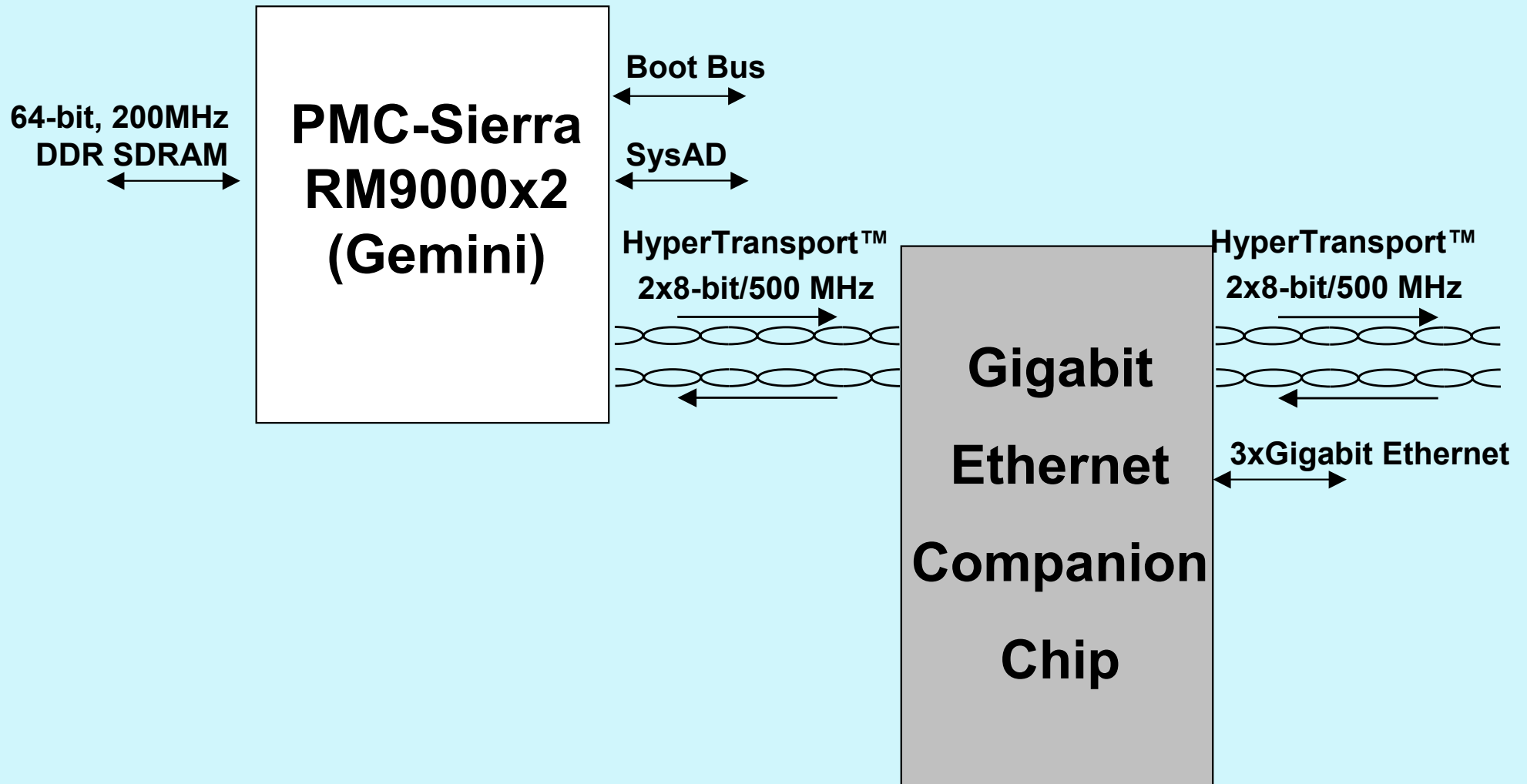


- 64bit, 66MHz PCI v2.2
- Two 8-bit, 533MHz HyperTransport™ ports
- 3.3V or 5V operation
- Daisy chain up to 15 devices
 - fairness algorithm to equitably share bandwidth
- All ports fully buffered

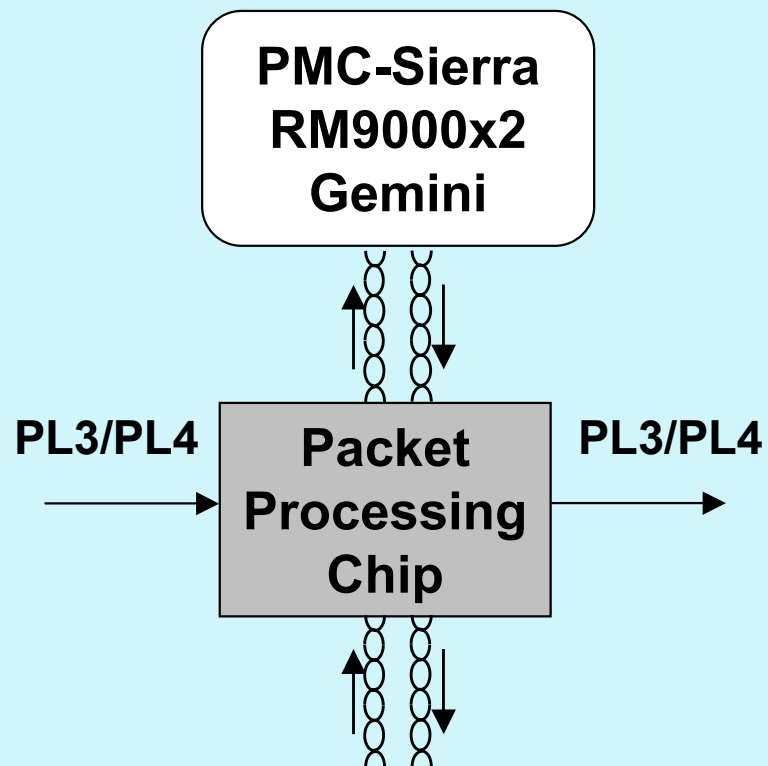
HyperTransport 4-Port Switch



Gigabit Ethernet Connectivity



HyperTransport Packet Processor Provides Data Plane Solution



- **PL3/PL4 Interface to Ethernet, Sonet**
- **Edge Router Solutions**
 - MPLS
 - FR – ATM
 - IPV6 Tunneling

Summary

- **The RM9000x2 Integrated Multiprocessor Architecture Requires a High Performance I/O Bus to Match its High Performance CPU Subsystem**
- **HyperTransport, With its High Bandwidth and PCI Support Provide the Ideal Solution**
- **Multiple HyperTransport Companion Chips Provide a Wide Range of System Solutions**